Amendments to the Specification:

Please replace the paragraph at page 8, lines 17-26 with the following amended paragraph:

After the precharge signal (PRECH) is transited from the ground voltage (VSS) to the boosting voltage (VPP), the decoded row address signals (DRA1, DRA_C2, DRA_C3) are transited from the ground voltage (VSS) to the supply voltage (VCC) and the decoded address signal (DRA_C4) is activated to the supply voltage (VCC) for a predetermined time interval. Then, the electrical potential of the node (NODE4) is transited from a high impedance state (HI-Z) to the negative voltage (VNEG) and the electrical potential of the node (NODE3) is rapidly transited from the boosting voltage (VPP) to the negative voltage (VNEG) ~~ground voltage (VSS)~~. As a result, the first main word line signal (MWE1) is quickly activated from the ground voltage (VSS) to the boosting voltage (VPP).

Please replace the paragraph at page 8, line 27 through page 9, line 5 with the following amended paragraph:

When the decoded row address signal (DRA_C4) is transited from the supply voltage (VCC) to the ground voltage (VSS), the decoded row address signal (DRA_C1) is transited from the ground voltage (VSS) to the supply voltage (VCC). Then, the electrical potential of the [[node]]nodes (NODE4 and NODE3) [[is]]are transited from the negative voltage (VNEG) to the ground voltage (VSS) and the ground voltage of the electrical potential of the [[node]]nodes (NODE4 and NODE3) [[is]]are maintained. Then, the ~~ground voltage (VSS) of the electrical potential of the node (NODE3) is maintained and the~~ activation state of the boosting voltage (VPP) of the first main word line signal (MWE1) is maintained.